# LH534P00A

## FEATURES

- 524,288 words $\times$ 8 bit organization
  (Byte mode)
  262,144 words $\times$ 16 bit organization
  (Word mode)

- Access time:  120 ns (MAX.)

- Power consumption:
  Operating:  357.5 mW (MAX.)
  Standby:  550 $\mu$W (MAX.)

- Static operation

- TTL compatible I/O

- Three-state outputs

- Single +5 V power supply

- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 $\times$ 18 mm$^2$ TSOP (Type I)

## DESCRIPTION

   The LH534P00A is a 4M-bit mask-programmable ROM organized as 524,288 $\times$ 8 bits (Byte mode) or 262,144 $\times$ 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS



40-PIN DIP
40-PIN SOP                                    TOP VIEW

| Pin | | Pin | |
|---|---|---|---|
| $A_{17}$ | 1 ● | 40 | $A_8$ |
| $A_7$ | 2 | 39 | $A_9$ |
| $A_6$ | 3 | 38 | $A_{10}$ |
| $A_5$ | 4 | 37 | $A_{11}$ |
| $A_4$ | 5 | 36 | $A_{12}$ |
| $A_3$ | 6 | 35 | $A_{13}$ |
| $A_2$ | 7 | 34 | $A_{14}$ |
| $A_1$ | 8 | 33 | $A_{15}$ |
| $A_0$ | 9 | 32 | $A_{16}$ |
| $\overline{\text{CE}}$ | 10 | 31 | $\overline{\text{BYTE}}$ |
| GND | 11 | 30 | GND |
| $\overline{\text{OE}}$ | 12 | 29 | $D_{15}/A_{-1}$ (LSB) |
| $D_0$ | 13 | 28 | $D_7$ |
| $D_8$ | 14 | 27 | $D_{14}$ |
| $D_1$ | 15 | 26 | $D_6$ |
| $D_9$ | 16 | 25 | $D_{13}$ |
| $D_2$ | 17 | 24 | $D_5$ |
| $D_{10}$ | 18 | 23 | $D_{12}$ |
| $D_3$ | 19 | 22 | $D_4$ |
| $D_{11}$ | 20 | 21 | $V_{CC}$ |
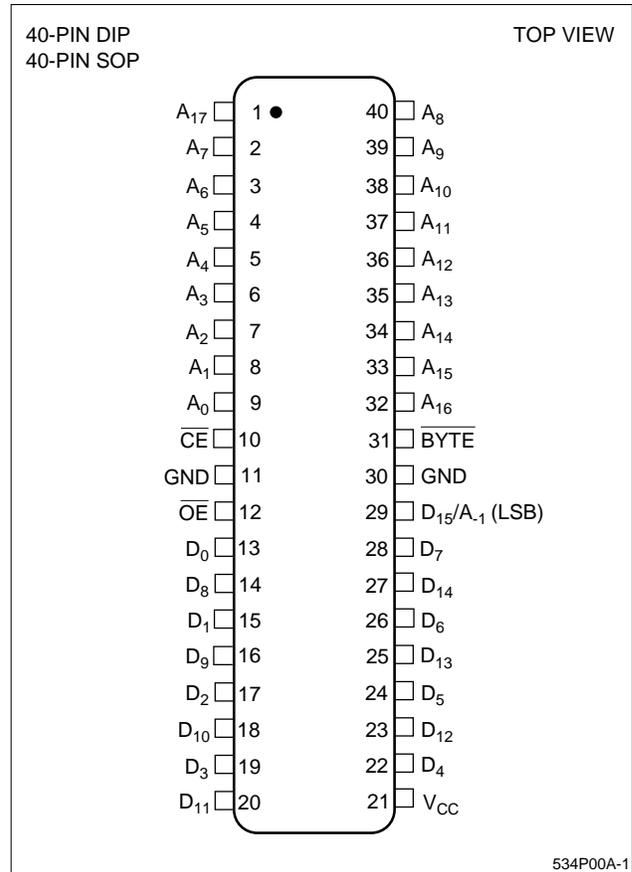
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**Figure 1.  Pin Connections for DIP and
SOP Packages**
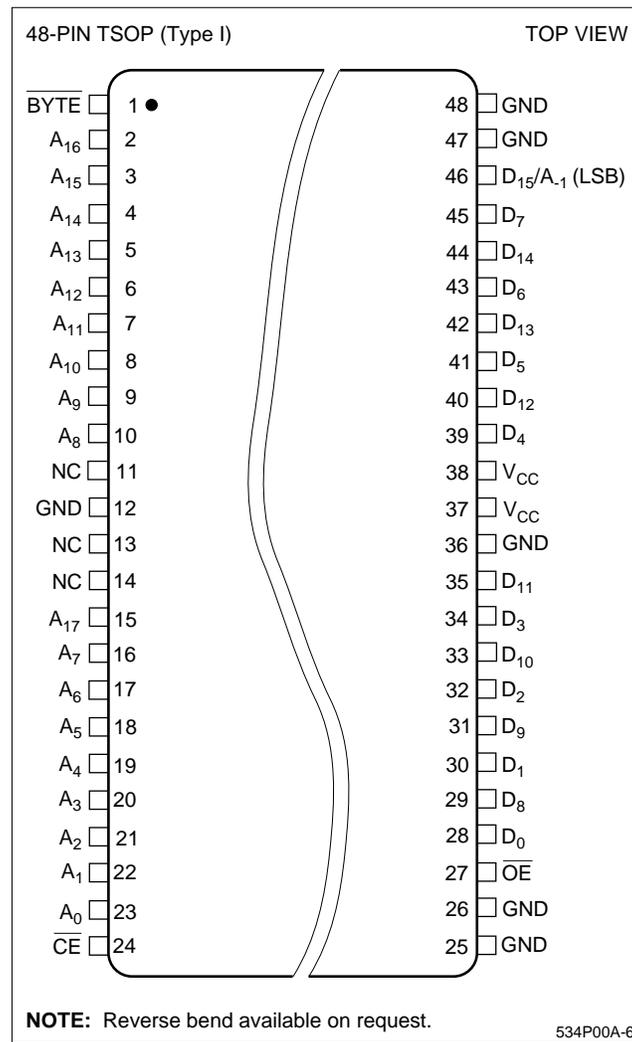
**Figure 2. Pin Connections for TSOP Package**

| | | | |
|---|---|---|---|
| $\overline{BYTE}$ | 1 ● | 48 | GND |
| $A_{16}$ | 2 | 47 | GND |
| $A_{15}$ | 3 | 46 | $D_{15}/A_{-1}$ (LSB) |
| $A_{14}$ | 4 | 45 | $D_7$ |
| $A_{13}$ | 5 | 44 | $D_{14}$ |
| $A_{12}$ | 6 | 43 | $D_6$ |
| $A_{11}$ | 7 | 42 | $D_{13}$ |
| $A_{10}$ | 8 | 41 | $D_5$ |
| $A_9$ | 9 | 40 | $D_{12}$ |
| $A_8$ | 10 | 39 | $D_4$ |
| NC | 11 | 38 | $V_{CC}$ |
| GND | 12 | 37 | $V_{CC}$ |
| NC | 13 | 36 | GND |
| NC | 14 | 35 | $D_{11}$ |
| $A_{17}$ | 15 | 34 | $D_3$ |
| $A_7$ | 16 | 33 | $D_{10}$ |
| $A_6$ | 17 | 32 | $D_2$ |
| $A_5$ | 18 | 31 | $D_9$ |
| $A_4$ | 19 | 30 | $D_1$ |
| $A_3$ | 20 | 29 | $D_8$ |
| $A_2$ | 21 | 28 | $D_0$ |
| $A_1$ | 22 | 27 | $\overline{OE}$ |
| $A_0$ | 23 | 26 | GND |
| $\overline{CE}$ | 24 | 25 | GND |

48-PIN TSOP (Type I)     TOP VIEW

**NOTE:** Reverse bend available on request.
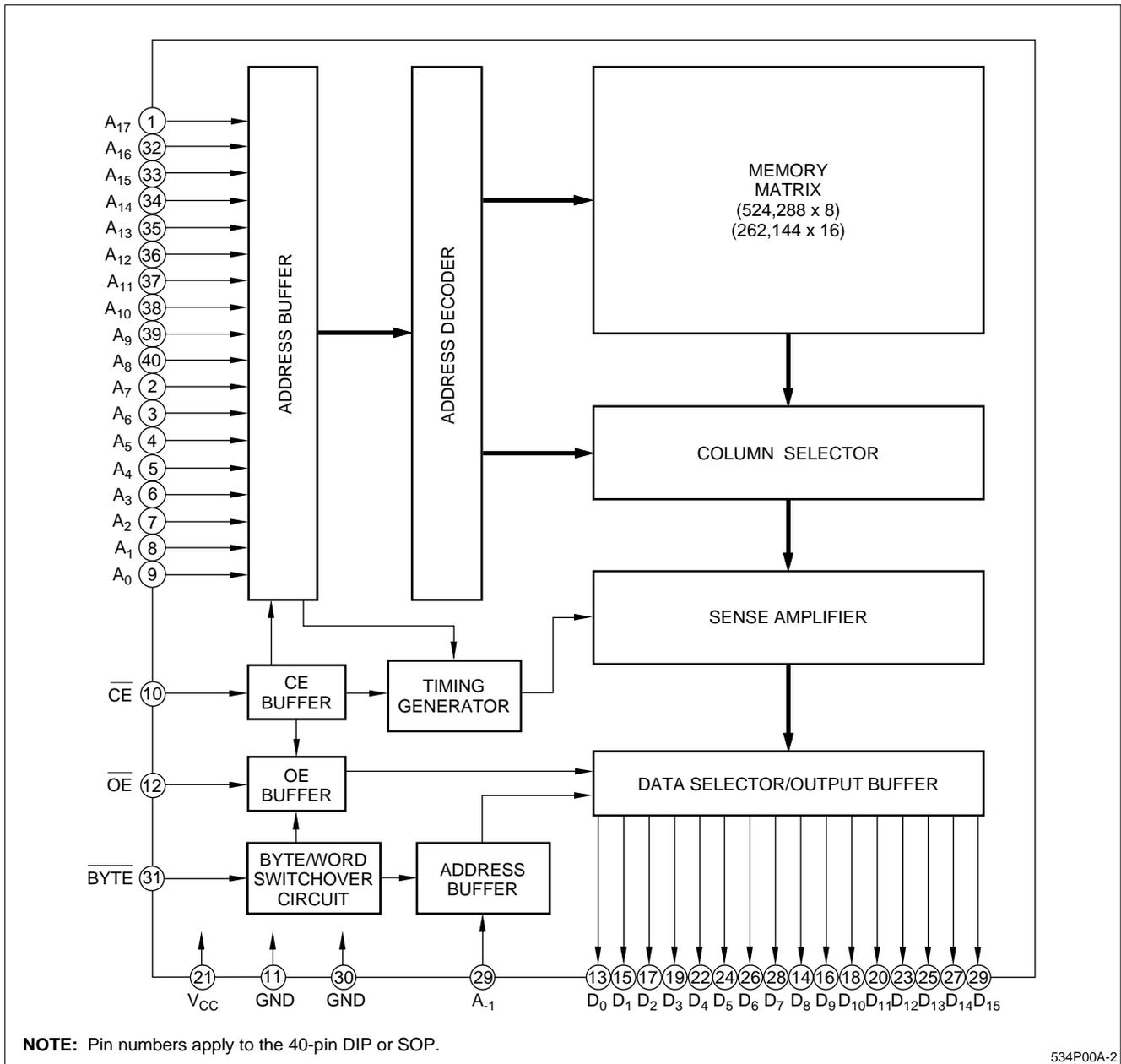
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**Figure 3. LH534P00A Block Diagram**

## PIN DESCRIPTION

| SIGNAL | PIN NAME | NOTE |
|---|---|---|
| $A_{-1}$ | Address input (BYTE mode) | 1 |
| $A_0 - A_{17}$ | Address input | |
| $D_0 - D_{15}$ | Data output | 1 |
| $\overline{BYTE}$ | Byte/word mode switch | 1 |

| SIGNAL | PIN NAME | NOTE |
|---|---|---|
| $\overline{CE}$ | Chip enable input | |
| $\overline{OE}$ | Output enable input | |
| $V_{CC}$ | Power supply (+5 V) | |
| GND | Ground | |

**NOTE:**

1. $D_{15}/A_{-1}$ pin becomes LSB address input ($A_{-1}$) when the bit configuration is set in byte mode, and data output ($D_{15}$) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

## TRUTH TABLE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{BYTE}$ | $A_{-1}$ | MODE | DATA OUTPUT | | SUPPLY CURRENT | NOTE |
|---|---|---|---|---|---|---|---|---|
| | | | | | $D_0 - D_7$ | $D_8 - D_{15}$ | | |
| H | X | X | X | Not selected | High-Z | High-Z | Standby ($I_{SB}$) | 1 |
| L | H | X | X | Not selected | High-Z | High-Z | Operating ($I_{CC}$) | |
| L | L | H | Input inhibit | Word | $D_0 - D_7$ | $D_8 - D_{15}$ | Operating ($I_{CC}$) | |
| L | L | L | L | Byte | $D_0 - D_7$ | High-Z | Operating ($I_{CC}$) | |
| L | L | L | H | Byte | $D_8 - D_{15}$ | High-Z | Operating ($I_{CC}$) | |

**NOTE:**
1. The input state of $\overline{BYTE}$ pin must not be changed during operation. The $\overline{BYTE}$ pin must be set to either HIGH or LOW.
   X = H or L

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | −0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | −0.3 to $V_{CC}$ + 0.3 | V |
| Output voltage | $V_{OUT}$ | −0.3 to $V_{CC}$ + 0.3 | V |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | −65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS  ($T_A$ = 0 to +70°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |

## DC CHARACTERISTICS  ($V_{CC}$ = 5 V $\pm$10%, $T_A$ = 0 to +70°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Input 'Low' voltage | $V_{IL}$ | | −0.3 | | 0.8 | V | |
| Input 'High' voltage | $V_{IH}$ | | 2.2 | | $V_{CC}$ + 0.3 | V | |
| Output 'Low' voltage | $V_{OL}$ | $I_{OL}$ = 2.0 mA | | | 0.4 | V | |
| Output 'High' voltage | $V_{OH}$ | $I_{OH}$ = −400 µA | 2.4 | | | V | |
| Input leakage current | $|I_{LI}|$ | $V_{IN}$ = 0 V to $V_{CC}$ | | | 10 | µA | |
| Output leakage current | $|I_{LO}|$ | $V_{OUT}$ = 0 V to $V_{CC}$ | | | 10 | µA | 1 |
| Operating current | $I_{CC1}$ | $t_{RC}$ = 120 ns | | | 65 | mA | 2 |
| | $I_{CC2}$ | $t_{RC}$ = 1 µs | | | 50 | | |
| | $I_{CC3}$ | $t_{RC}$ = 120 ns | | | 60 | mA | 3 |
| | $I_{CC4}$ | $t_{RC}$ = 1 µs | | | 45 | | |
| Standby current | $I_{SB1}$ | $\overline{CE}$ = $V_{IH}$ | | | 3 | mA | |
| | $I_{SB2}$ | $\overline{CE}$ = $V_{CC}$ − 0.2 V | | | 100 | µA | |
| Input capacitance | $C_{IN}$ | f = 1 MHz | | | 10 | pF | |
| Output capacitance | $C_{OUT}$ | $T_A$ = 25°C | | | 10 | pF | |

**NOTES:**
1. $\overline{CE}/\overline{OE}$ = $V_{IH}$
2. $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE}$ = $V_{IL}$, outputs open
3. $V_{IN}$ = ($V_{CC}$ − 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

## AC CHARACTERISTICS  ($V_{CC}$ = 5 V $\pm$10%, $T_A$ = 0 to +70°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 120 | | | ns | |
| Address access time | $t_{AA}$ | | | 120 | ns | |
| Chip enable access time | $t_{ACE}$ | | | 120 | ns | |
| Output enable delay time | $t_{OE}$ | | | 60 | ns | |
| Output hold time | $t_{OH}$ | 5 | | | ns | |
| CE to output in High-Z | $t_{CHZ}$ | | | 60 | ns | 1 |
| OE to output in High-Z | $t_{OHZ}$ | | | 60 | ns | |

**NOTE:**
1.  This is the time required for the outputs to become high-impedance.

## AC TEST CONDITIONS

| PARAMETER | RATING |
|---|---|
| Input voltage amplitude | 0.4 V to 2.6 V |
| Input rise/fall time | 10 ns |
| Input/output reference level | 1.5 V |
| Output load condition | 1TTL + 100 pF |

## CAUTION

   To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the $V_{CC}$ pin and the GND pin.
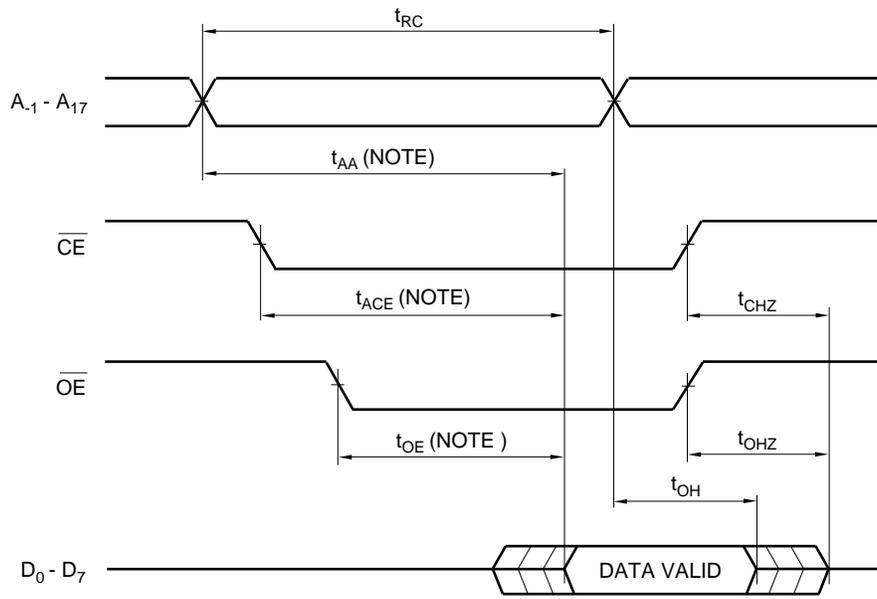
NOTE: The output data becomes valid when the last intervals, $t_{AA}$, $t_{ACE}$, or $t_{OE}$, have concluded.

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**Figure 4.  Byte Mode ($\overline{\text{BYTE}}$ = $V_{IL}$)**
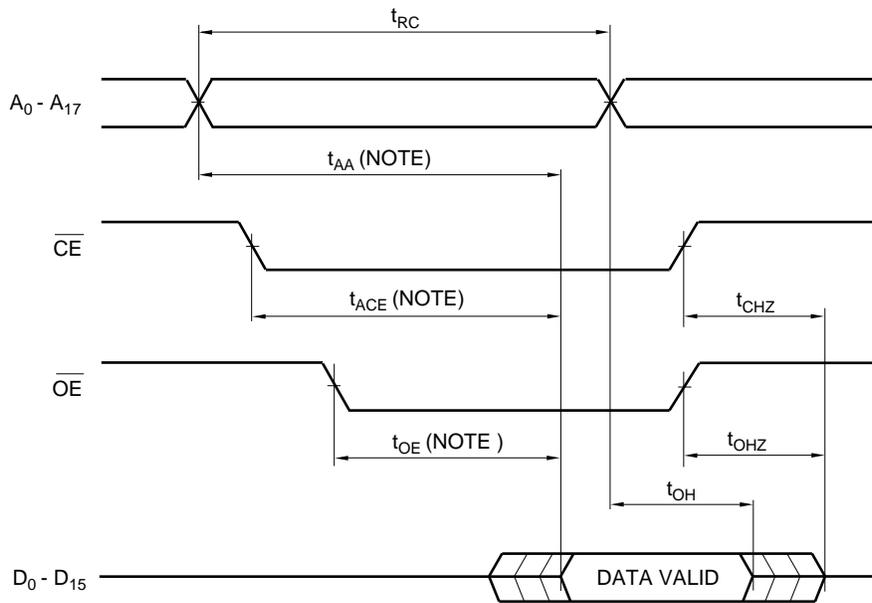


NOTE: The output data becomes valid when the last intervals, $t_{AA}$, $t_{ACE}$, or $t_{OE}$, have concluded.

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**Figure 5.  Word Mode ($\overline{\text{BYTE}}$ = $V_{IH}$)**

## PACKAGE DIAGRAMS

### 40DIP (DIP040-P-0600)



**40-pin, 600-mil DIP**

### 40SOP (SOP040-P-0525)



**40-pin, 525-mil SOP**

**48TSOP (TSOP048-P-1218)**
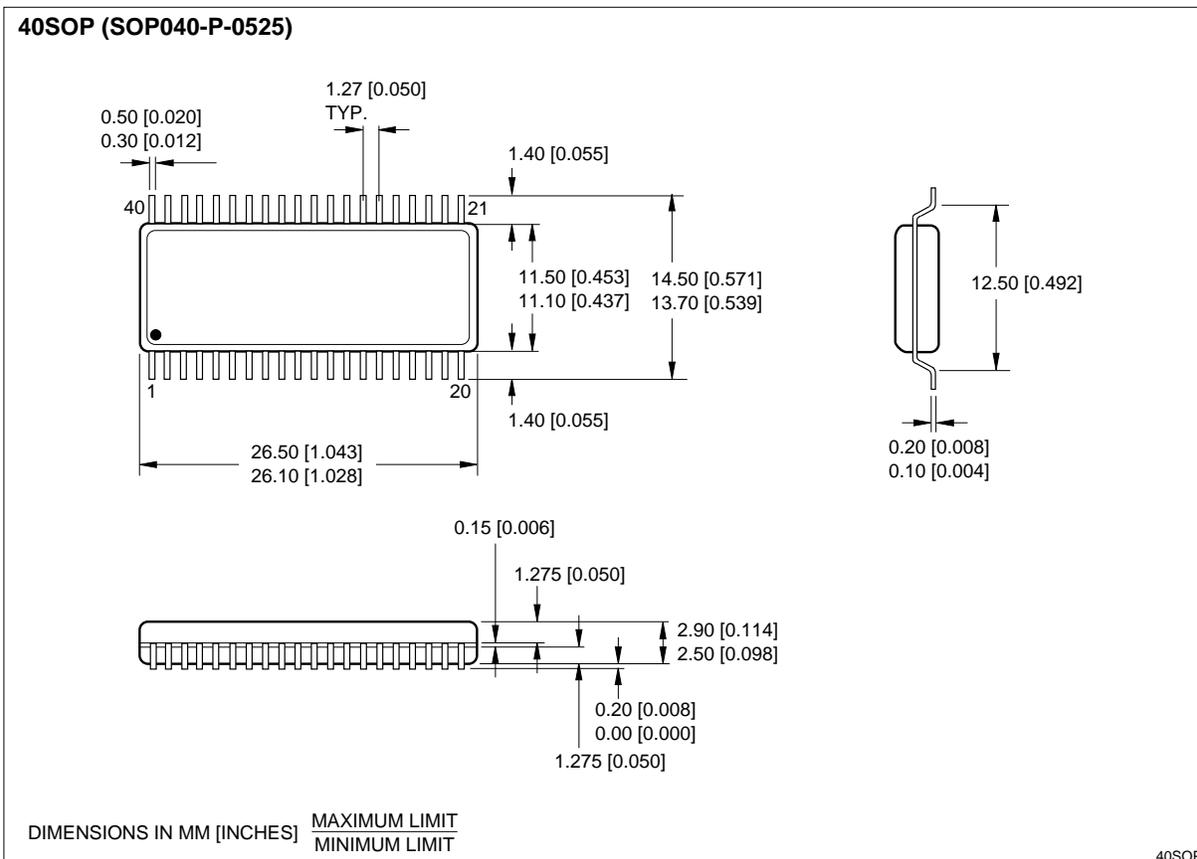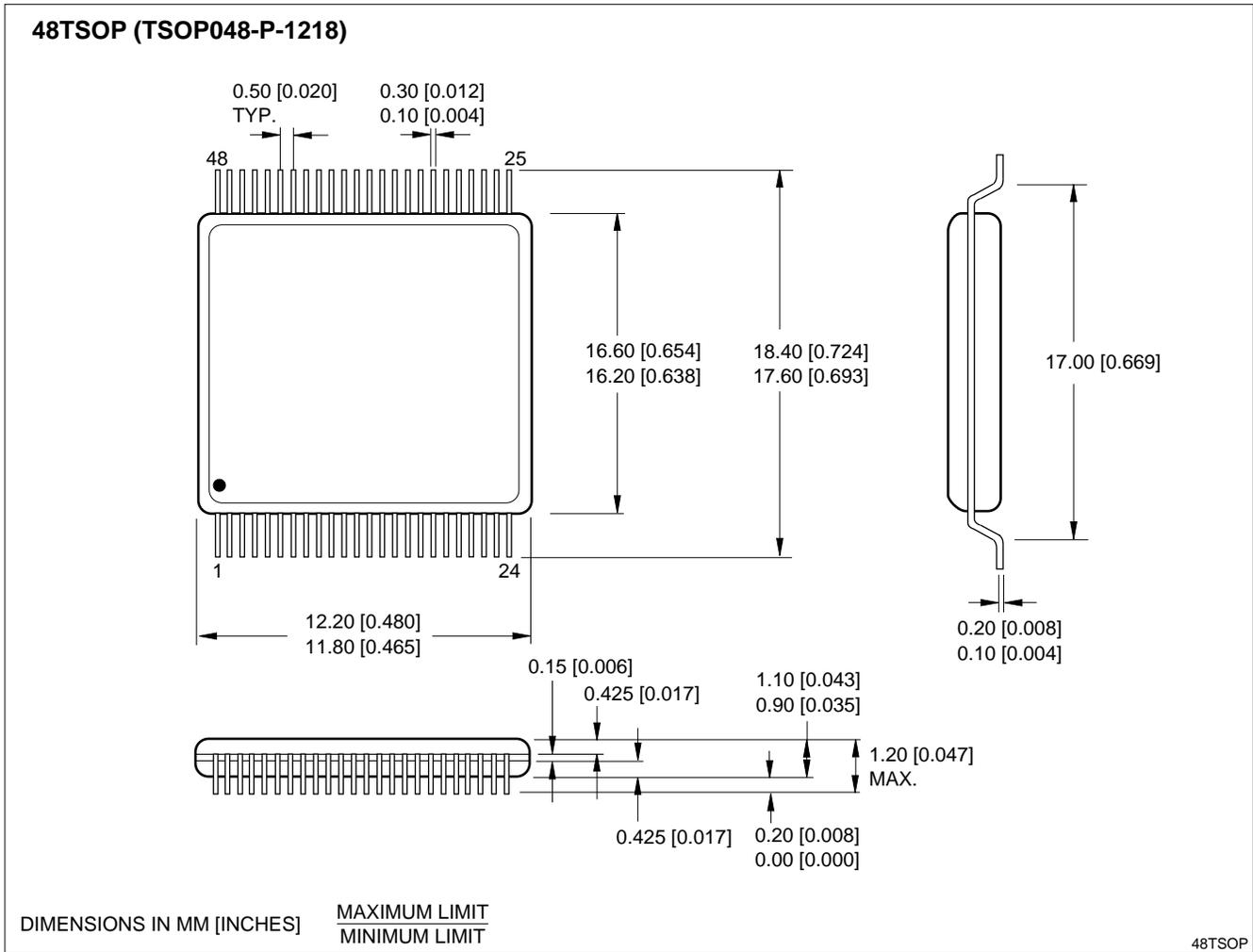


**48-pin, 12 × 18 mm² TSOP (Type I)**

## ORDERING INFORMATION



LH534P00A         X
Device Type      Package

D    40-pin, 600-mil DIP (DIP040-P-0600)
N    40-pin, 525-mil SOP (SOP040-P-0525)
T    48-pin, 12 x 18 mm² TSOP (Type I) (TSOP048-P-1218)
TR   48-pin, 12 x 18 mm² TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM

**Example:** LH534P00AD (CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM, 40-pin, 600-mil DIP)

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